



CARRIER CLOCK RECOVERY USING PLL AND COSTAS LOOP TRAINER MODEL - CK GEN 100

This trainer has been designed with a view to provide practical & experimental knowledge of the process of Carrier clock regeneration from received data stream in digital system on single PCB.

SPECIFICATIONS

1. Power supply requirement : 230V AC, 50 Hz.
2. Built in IC based power supply.
3. On Board Digital generator -TTL
Bit Clock Frequency : 70 to 90 KHz
4. Data transmission by PSK method.
5. Clock recovery by PLL and Costas loop methods
6. Standard Accessories : A Training Manual
Connecting Patch cords.

EXPERIMENTS

1. To understand Block diagram and working principle
2. To study theory of digital transmission.
3. To regenerate bit clock.
4. To synchronize the word clock.
5. To observe the effect of asynchronies on analog waveforms.
6. To understand - S/H - Integrate & Dump process.

In keeping view of SIGMA policy of continuous development and improvement, the Specifications may be changed without prior notice or obligation.

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